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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/763,868	02/28/2001	Michel Hazard	T2146-906833	3510

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EXAMINER	
TRAN, TONGOC	

ART UNIT	PAPER NUMBER
2134	

DATE MAILED: 09/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/763,868	HAZARD, MICHEL	
	Examiner	Art Unit	
	Tongoc Tran	2134	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 February 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/28/2001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to applicant's preliminary amendment filed on 2/28/2001. Claims 1-19 have been cancelled. Claims 20-38 have been added. Claims 20-38 are pending.

Information Disclosure Statement

2. The information disclosure statement filed on 2/28/2001 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because there are no translations provided for the foreign prior art. It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609 ¶ C(1).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 20-23, 26-34 and 37-38 are rejected under 35 U.S.C. 102(b) as being anticipated by Holtey (U.S. Patent No. 5,442,704).

In respect to claim 20, Holtey discloses a method for protecting the processing of sensitive information in a security module having a monolithic structure, information processing means (31) and storage means for storing (32,33) information capable of being processed by said processing means, comprising the following steps (see, Abstract):

selecting a piece of sensitive information stored in the storage means;

determining a specific condition for the integrity of said information;

reading the information and transmitting it to the processing means for processing (see col. 3, line 15 – col. 4, line 29);

processing the information and verifying during processing that the specific condition is satisfied; and disabling processing of the information if the specific condition is not satisfied (see col. 4, lines 30-49).

In respect to claim 21, Holtey discloses the method according to claim 20, wherein the information is an operation code read in the storage means (32, 33), the operation code being contained in a table having a content determined during the manufacture of the security module, and the specific condition for the integrity of the information being the value of the information is equal to one of several set values (see col. 3, line 15 – col. 4, line 29).

In respect to claim 22, Holtey discloses the method according to claim 21, wherein the operation code to be processed is coded in the form of data bits and said bits do not all have the same binary value (see col. 3, lines 59-68).

In respect to claim 23, Holtey discloses the method according to claim 20, wherein the specific step of determining the condition for the integrity of said information comprises checking a calculated or first piece of integrity data using the information read in the storage means (32, 33) during the reading of the information and transmitting the first piece of integrity data to the processing means, and calculating a second piece of integrity data by the processing means from the information received and checking for equality between the first and second pieces of integrity data (see col. 3, lines 15-58).

In respect to claim 26, Holtey discloses the method according to claim 20, wherein the disabling of the processing of the information is performed by a microprogrammed instruction (see col. 4, lines 4-49).

In respect to claim 27, Holtey discloses the method according to claim 26, wherein the microprogrammed instruction performs the following steps:

writing a piece of disable data into a nonvolatile location of the storage means (32, 33); and disabling the processing of the information (see col. 3, lines 15-27 and col. 4, lines 4-49).

In respect to claim 28, Holtey discloses the method according to claim 27 further comprising reading by the processing means (31) a nonvolatile location of the storage

means (32, 33) upon power up of said module and disabling the module if a value read at this location does not match (see col. 4, lines 30-49 and col. 12, lines 50-60).

In respect to claim 29, the claim limitation is a system claim that is substantially similar to method claim 1. Therefore, claim 29 are rejected based on the similar rationale.

In respect to claim 30, Holtey discloses a security module according to claim 29, wherein the processing means (31) execute instructions corresponding to operation codes extracted from a table, characterized in that the table comprises a forbidden instruction value (see col. 3, lines 15-27).

In respect to claim 31, the claim limitation is a system claim that is substantially similar to method claim 23. Therefore, claim 31 is rejected based on the similar rationale.

In respect to claim 32, Holtey discloses the security module according to claim 29, wherein the processing means (31) execute instructions corresponding to operation codes extracted from a table, the security module comprising a means for reading an operation code and a disabling means activated during the reading of a forbidden 5 operation code (see col. 3, lines 28-58).

In respect to claim 33, Holtey discloses the security module according to claim 32, wherein the disabling means comprise a means for irreversibly writing an indicator into the storage 3 means (32, 33), and a means for reading said indicator during the next power-up of the module (see col. 4, lines 30-49 and col. 2, lines 50-68).

In respect to claim 34, A security module according to claim 29, comprising parity

generators (7, 8) cooperating with the storage means, parity generators (11) cooperating with the processing means, and a comparator connected to each of the parity generators and capable of inducing an interrupt in the processing means (see col. 2, line 57 – col. 3, line 3).

In respect to claim 37, the claim limitation is a system claim that is substantially similar to method claim 26. Therefore, claim 37 is rejected based on the similar rationale.

In respect to claim 38, Holtey discloses the security module according to claim 29, characterized in that the security module is a microcircuit card (see col. 3, lines 15-27).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 24-25 and 35-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Holtey (U.S. Patent No. 5,442,704) in view of Hogg et al. (U.S. Patent No. 4,281,216).

In respect to claims 24-25, Holtey discloses the method according to claim 23. Holtey does not disclose but Hogg discloses a piece of integrity data is calculated from

at least one piece of calculation data whose value varies as a function of time or varies randomly (Hogg, col. 9, lines 19-48). It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the function of time with a pseudorandom number generator to varies a value taught by Hogg with Holtey's teaching of secure memory card with programmed controlled of security access for the benefit that there is no human knowledge of the generated keys (Hogg, col. 19-32).

In respect to claims 35-36, the claim limitations are system claims that are substantially similar to method claims 24-25. Therefore, claims 35-36 are rejected based on the similar rationale.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

-Hansen et al. Disclose a system for performing DMA transfers where an interrupt request signal is generated based on the value of the last of a plurality of data bits transmitted.

-Takahira discloses an IC card having Internal error checking capacity.

-Thompson et al. Disclose a system and methods for continually and retrieving interactive video information.

-Klingler discloses an integrated circuit comprising means to halt the performance of a program of instructions when a combination of breakpoints is verified.

-Geronimi et al. Disclose a system for monitoring abnormal integrated operating conditions and causing selective microprocessor interrupts.

-Sakaki et al. Disclose memory data protection circuit.

-Nakatsyama discloses device for verifying use qualifications.

-Edwards et al. Disclose a fault tolerant multiprocessor computer system.

-Ugon discloses a single chip microprocessor with on-chip modifiable memory.

-Nassor discloses method for modifying code sequences and related device.

-Iijima discloses a portable electronic device with means for checking data validity during read-out.

-Pawloski discloses a shared bus in-circuit emulator system and method.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tongoc Tran whose telephone number is (703) 305-7690. The examiner can normally be reached on 8:30-5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gregory A. Morse can be reached on (703) 308-4789. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner: Tongoc Tran
Art Unit: 2134

TT

August 31, 2004

GREGORY MORSE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100